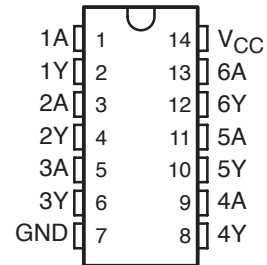● **Dependable Texas Instruments Quality and Reliability**

description/ordering information

These devices contain six independent inverters.

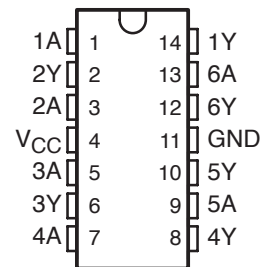**SN5404 . . . J PACKAGE**
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
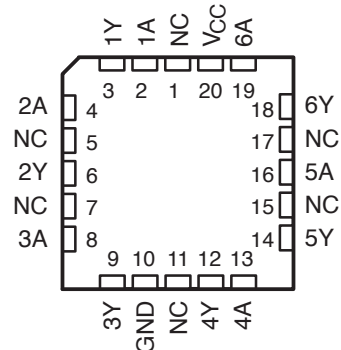**SN74LS04 . . . D, DB, N, OR NS PACKAGE**
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

SN5404 . . . W PACKAGE
(TOP VIEW)

1A	1	14	1Y
2Y	2	13	6A
2A	3	12	6Y
V_{CC}	4	11	GND
3A	5	10	5Y
3Y	6	9	5A
4A	7	8	4Y

SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Y (3), 1A (2), NC (1), V_{CC} (20), 6A (19)

Left pins: 2A (4), NC (5), 2Y (6), NC (7), 3A (8)

Right pins: 6Y (18), NC (17), 5A (16), NC (15), 5Y (14)

Bottom pins: 3Y (9), GND (10), NC (11), 4Y (12), 4A (13)

NC – No internal connection

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ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC – D	Tube	SN7404D	7404
		Tape and reel	SN7404DR	
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP – NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP – DB	Tape and reel	SN74LS04DBR	LS04
−55°C to 125°C	CDIP – J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP – W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC – FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines
   are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

![Texas Instruments logo] **TEXAS INSTRUMENTS**
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)
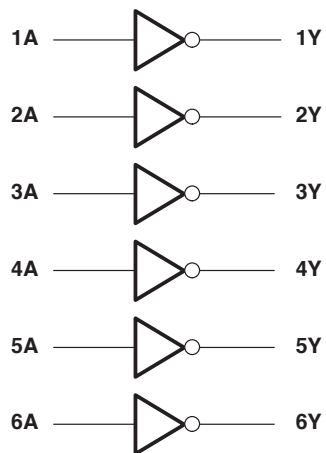
$Y = \overline{A}$

schematics (each gate)

'04

'LS04

'S04
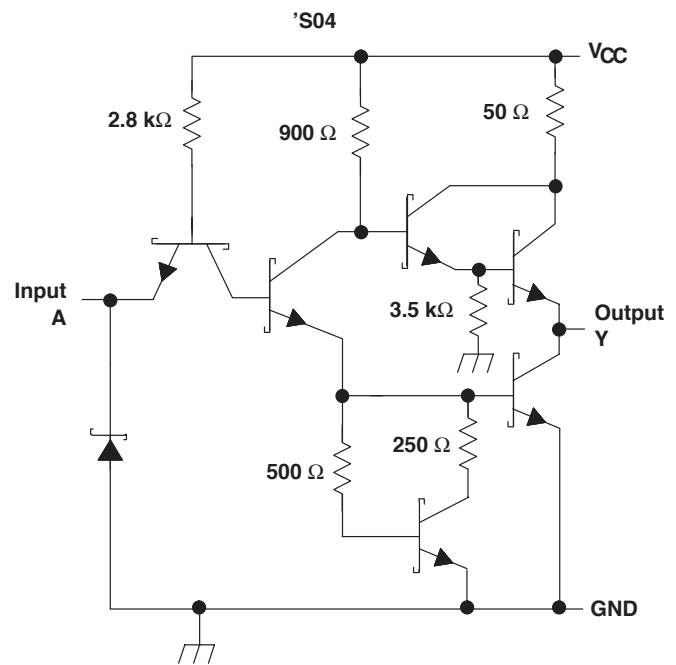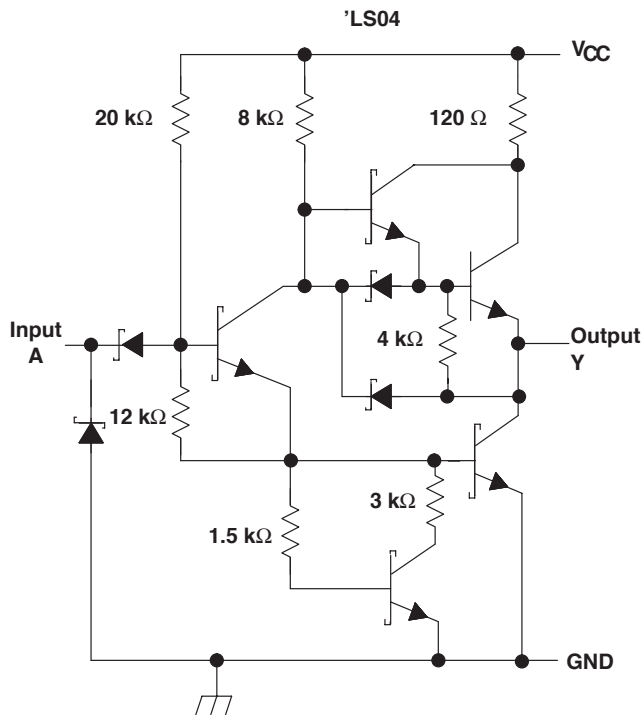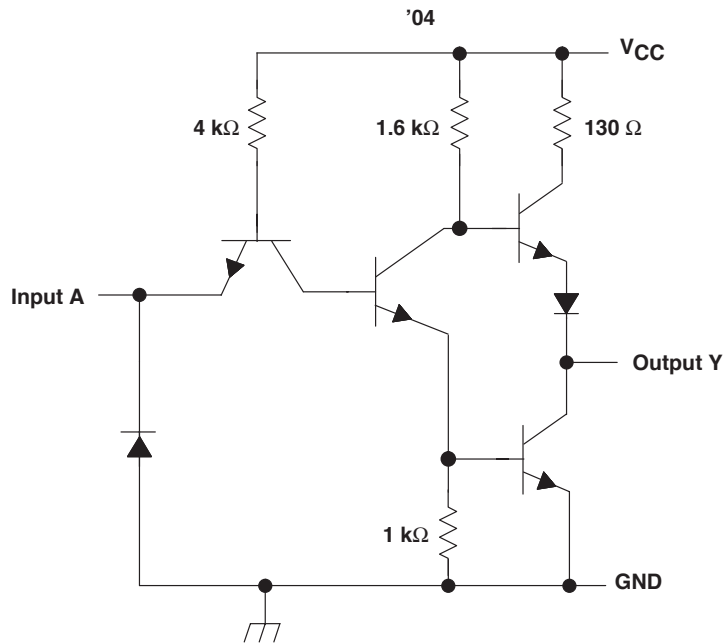
Resistor values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage, V_I: '04, 'S04 .... 5.5 V
                                  'LS04 .... 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
                                                                            DB package .... 96°C/W
                                                                            N package .... 80°C/W
                                                                            NS package .... 76°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. Voltage values are with respect to network ground terminal.
           2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		SN5404			SN7404			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V			40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V		6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V		18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN5404 SN7404			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω,	C_L = 15 pF		12	22	ns
t_{PHL}						8	15	

recommended operating conditions (see Note 3)

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54LS04 SN74LS04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ,	C_L = 15 pF		9	15	ns
t_{PHL}						10	15	

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recommended operating conditions (see Note 3)

		SN54S04			SN74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]			SN54S04			SN74S04			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
I_{OS}[§]	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			15	24		15	24	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			30	54		30	54	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S04 SN74S04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES
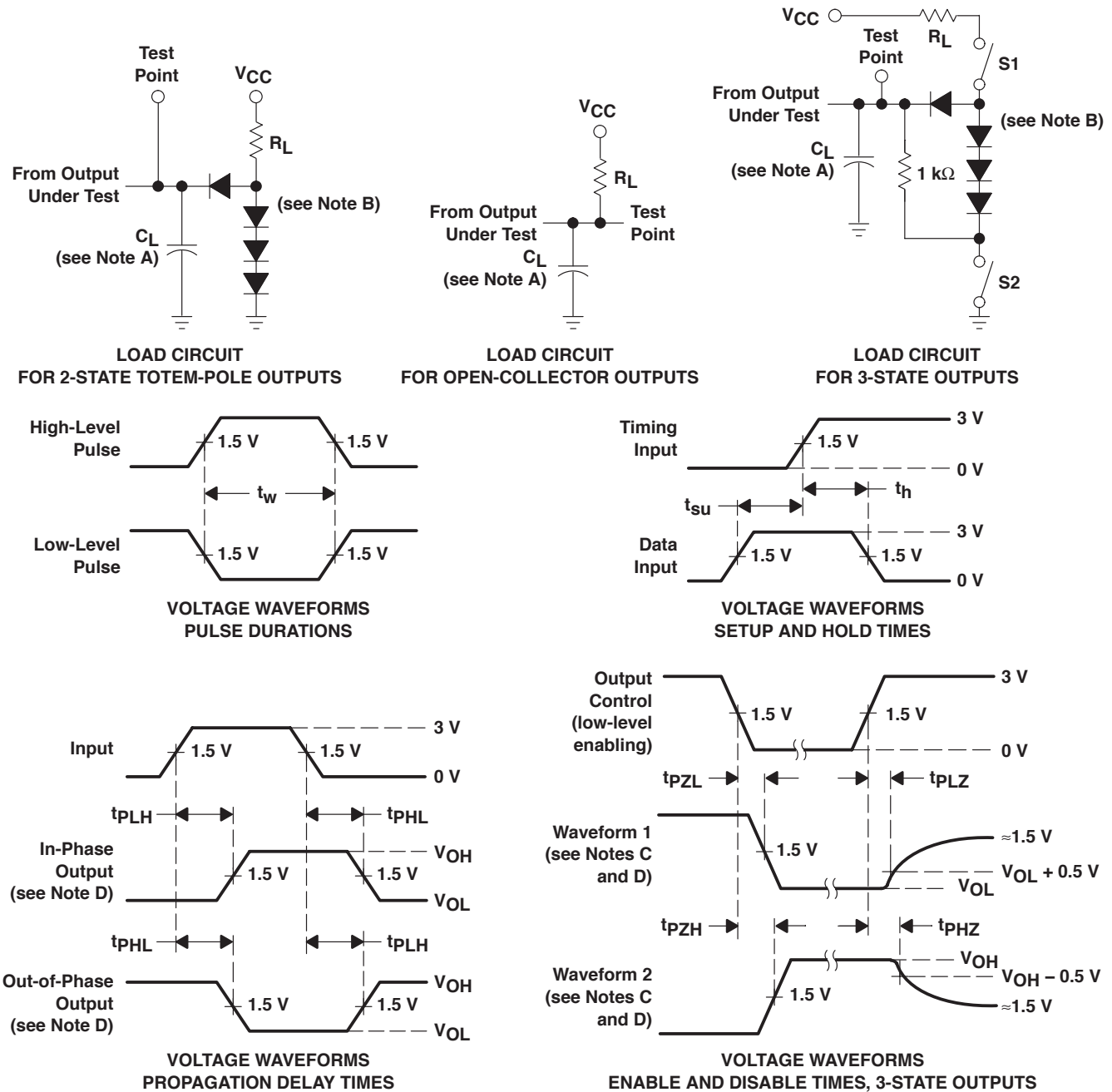
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω; t_r and t_f ≤ 7 ns for Series 54/74 devices and t_r and t_f ≤ 2.5 ns for Series 54S/74S devices.
F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES

Test Point

V$_{CC}$

R$_L$

From Output Under Test

(see Note B)

C$_L$
(see Note A)

**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**

V$_{CC}$

R$_L$

From Output Under Test

Test Point

C$_L$
(see Note A)

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

V$_{CC}$

R$_L$

Test Point

S1

From Output Under Test

(see Note B)

C$_L$
(see Note A)

5 kΩ

S2

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

High-Level Pulse   1.3 V   1.3 V

t$_w$

Low-Level Pulse   1.3 V   1.3 V

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

Timing Input   1.3 V   3 V   0 V

t$_{su}$ t$_h$

Data Input   1.3 V   1.3 V   3 V   0 V

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Input   1.3 V   1.3 V   3 V   0 V

t$_{PLH}$ t$_{PHL}$

In-Phase Output
(see Note D)   1.3 V   1.3 V   V$_{OH}$ V$_{OL}$

t$_{PHL}$ t$_{PLH}$

Out-of-Phase Output
(see Note D)   1.3 V   1.3 V   V$_{OH}$ V$_{OL}$

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

Output Control (low-level enabling)   1.3 V   1.3 V   3 V   0 V

t$_{PZL}$ t$_{PLZ}$

Waveform 1
(see Notes C and D)   1.3 V   ≈1.5 V   V$_{OL}$ + 0.5 V   V$_{OL}$

t$_{PZH}$ t$_{PHZ}$

Waveform 2
(see Notes C and D)   1.3 V   V$_{OH}$ V$_{OH}$ − 0.5 V   ≈1.5 V

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C$_L$ includes probe and jig capacitance.
   B. All diodes are 1N3064 or equivalent.
   C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   D. S1 and S2 are closed for t$_{PLH}$, t$_{PHL}$, t$_{PHZ}$, and t$_{PLZ}$; S1 is open and S2 is closed for t$_{PZH}$; S1 is closed and S2 is open for t$_{PZL}$.
   E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
   F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z$_O$ ≈ 50 Ω, t$_r$ ≤ 1.5 ns, t$_f$ ≤ 2.6 ns.
   G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms