Features

- Fast read access time – 45ns
- Low-power CMOS operation
  - 100µA max standby
  - 30mA max active at 5MHz
- JEDEC standard packages
  - 40-lead PDIP
  - 44-lead PLCC
- Direct upgrade from 512K (Atmel® AT27C516) EPROM
- 5V ± 10% power supply
- High-reliability CMOS technology
  - 2000V ESD protection
  - 200mA latchup immunity
- Rapid programming algorithm – 100µs/word (typical)
- CMOS- and TTL-compatible inputs and outputs
- Integrated product identification code
- Industrial and automotive temperature ranges
- Green (Pb/halide-free) packaging option

1Mb (64K x 16) One-time Programmable Read-only Memory

Atmel AT27C1024

1. Description

The Atmel AT27C1024 is a low-power, high-performance 1,048,576-bit, one-time programmable, read-only memory (OTP EPROM) organized as 64K by 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 45ns, eliminating the need for speed reducing WAIT states. The x16 organization makes this part ideal for high-performance, 16- and 32-bit microprocessor systems.

In read mode, the AT27C1024 typically consumes 15mA. Standby mode supply current is typically less than 10µA.

The AT27C1024 is available in industry-standard, JEDEC-approved, one-time programmable (OTP) PDIP and PLCC packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

With high-density, 64K word storage capability, the AT27C1024 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

The AT27C1024 has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/word. The integrated product identification code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

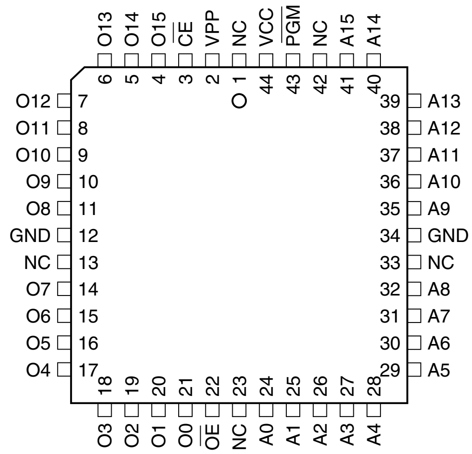
0019N–EPROM–4/11

2. Pin configurations

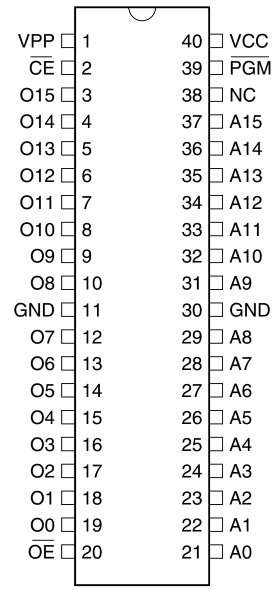
Pin name	Function
A0 - A15	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program strobe
NC	No connect

Note: Both GND pins must be connected.

44-lead PLCC
Top view



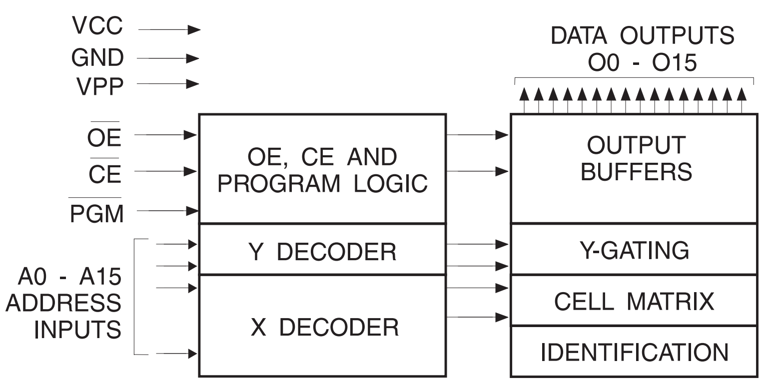
40-lead PDIP
Top view



3. System considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a 0.1µF, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Figure 3-1. Block diagram



4. Absolute maximum ratings*

Temperature under bias	-55°C to + 125°C
Storage temperature	-65°C to + 150°C
Voltage on any pin with respect to ground	-2.0V to + 7.0V[(1)]
Voltage on A9 with respect to ground	-2.0V to + 14.0V[(1)]
V_{PP} supply voltage with respect to ground	-2.0V to + 14.0V[(1)]

*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to +7.0V for pulses of less than 20ns.

5. DC and AC characteristics

Table 5-1. Operating modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	PGM	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X[(1)]	Ai	X	D_{OUT}
Output disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X[(5)]	High Z
Rapid program[(2)]	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product identification[(4)]	V_{IL}	V_{IL}	X	A9 = V_H[(3)] A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC}	Identification code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the manufacturer's identification word and high (V_{IH}) to select the device code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

Table 5-2. DC and AC operating conditions for read operation

		Atmel AT27C1024	
		-45	-70
Operating temp. (case)	Ind.	-40°C - 85°C	-40°C - 85°C
	Auto.		
V_{CC} power supply		5V ± 10%	5V ± 10%

Table 5-3. DC and operating characteristics for read operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input load current	V_{IN} = 0V to V_{CC}	Ind.		±1	µA
			Auto.		±5	µA
I_{LO}	Output leakage current	V_{OUT} = 0V to V_{CC}	Ind.		±5	µA
			Auto.		±10	µA
I_{PP1}[2]	V_{PP}[1] read/standby current	$V_{PP} = V_{CC}$			10	µA
I_{SB}	V_{CC}[1] standby current	I_{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} active current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE} = V_{IL}$			30	mA
V_{IL}	Input low voltage			-0.6	0.8	V
V_{IH}	Input high voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = -400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

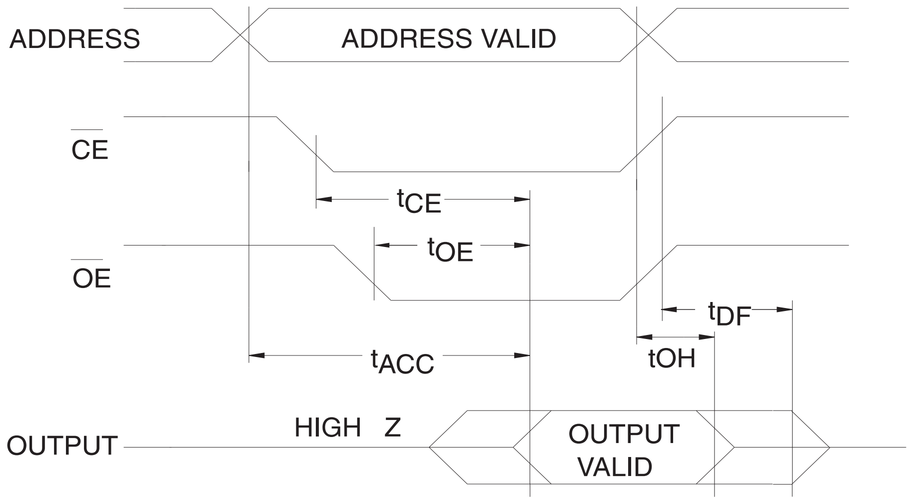
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

Table 5-4. AC characteristics for read operation

Symbol	Parameter	Condition	Atmel AT27C1024				Units
			-45		-70		
			Min	Max	Min	Max	
t_{ACC}[1]	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		45		70	ns
t_{CE}[1]	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		45		70	ns
t_{OE}[1]	$\overline{OE}$ to output delay	$\overline{CE} = V_{IL}$		20		25	ns
t_{DF}[1]	$\overline{OE}$ or $\overline{CE}$ high to output float, whichever occurred first			20		25	ns
t_{OH}	Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		ns

Note: 1. See AC waveforms for read operation.

Figure 5-1. AC waveforms for read operation[1]



Notes: 1. Timing measurement reference level is 1.5V for -45. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.

2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled, and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Table 5-5. Pin capacitance

f = 1MHz, T = 25°C[1]

Symbol	Typ	Max	Units	**Conditions**
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.

Figure 5-2. Input test waveforms and measurement levels

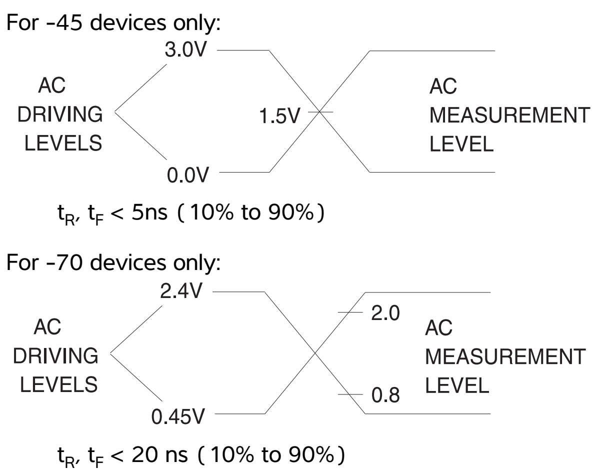
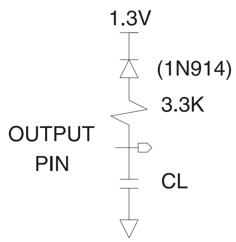
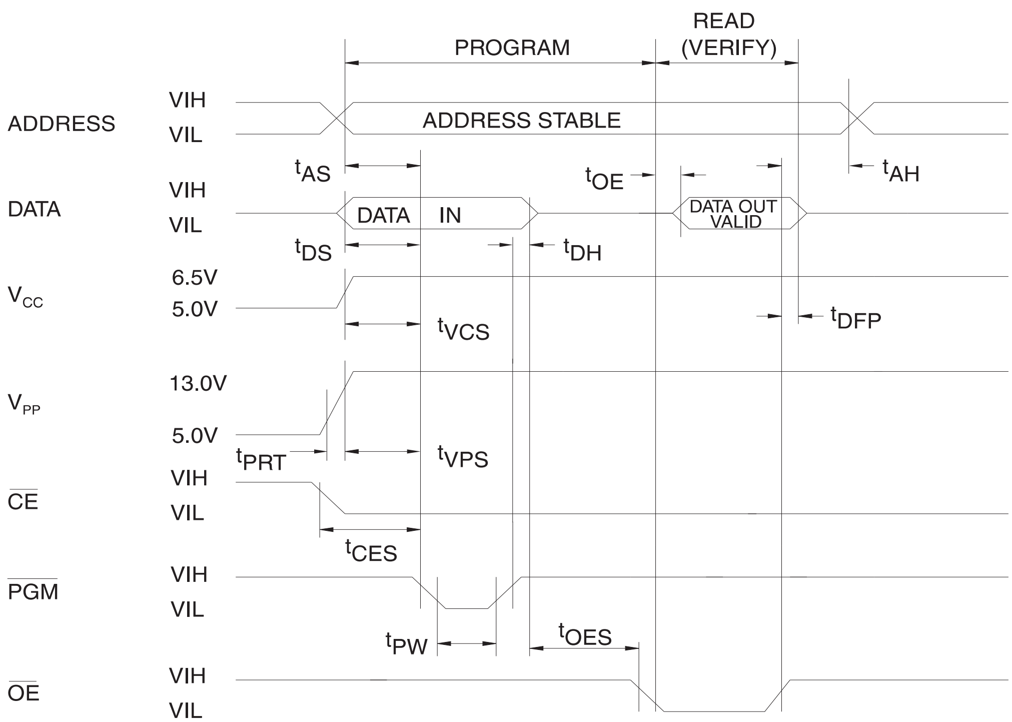


Figure 5-3. Output test load



Note: 1. C_L = 100pF including jig capacitance, except -45 devices, where C_L = 30pF.

Figure 5-4. Programming waveforms[1]



Notes: 1. The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

3. When programming the Atmel AT27C1024, a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

Table 5-6. DC programming characteristics

$T_A = 25 \pm 5°C, V_{CC} = 6.5 \pm 0.25V, V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test conditions	Limits		Units
			Min	Max	
I_{LI}	Input load current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input low level		-0.6	0.8	V
V_{IH}	Input high level		2.0	$V_{CC} + 0.1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400µA$	2.4		V
I_{CC2}	V_{CC} supply current (program and verify)			50	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 product identification voltage		11.5	12.5	V

Table 5-7. AC programming characteristics

$T_A = 25 \pm 5°C, V_{CC} = 6.5 \pm 0.25V, V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address setup time		2		µs
t_{CES}	$\overline{CE}$ setup time		2		µs
t_{OES}	$\overline{OE}$ setup time	Input rise and fall times (10% to 90%) 20ns	2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time	Input pulse levels 0.45V to 2.4V	0		µs
t_{DH}	Data hold time		2		µs
t_{DFP}	$\overline{OE}$ high to output float delay[2]	Input timing reference level 0.8V to 2.0V	0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{PW}	$\overline{PGM}$ program pulse width[3]	Output timing reference level 0.8V to 2.0V	95	105	µs
t_{OE}	Data valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} pulse rise time during programming		50		ns

Notes:
1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
3. Program pulse width tolerance is 100µsec ± 5%.

Table 5-8. The Atmel AT27C1024 integrated product identification code

Codes	Pins										Hex data
	A0	O15-O8	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device type	1	0	1	1	1	1	0	0	0	1	00F1

6. Rapid programming algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.

Figure 6-1. Rapid programming algorithm