Name: _____

Read each question carefully before answering. Answer all parts. Show all work, calculations, and/or reasoning, otherwise no points will be awarded. Properly labeled loops must be shown on K-maps. Point values are as indicated.

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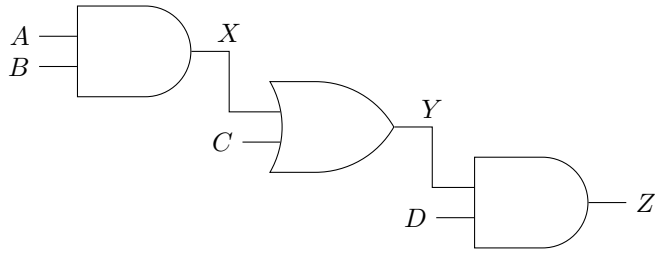
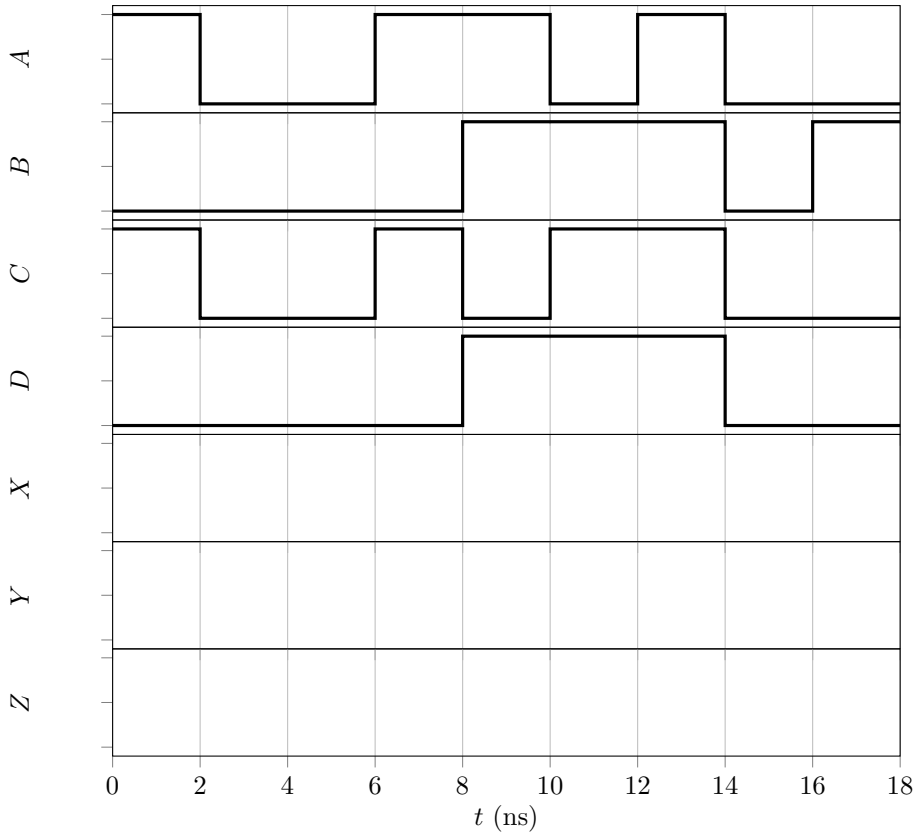
1. (25 points) Given the following circuit diagram, fill out the timing diagram for X, Y and Z. Each AND gate has a delay of 2 ns, and each OR gate has a delay of 1 ns.

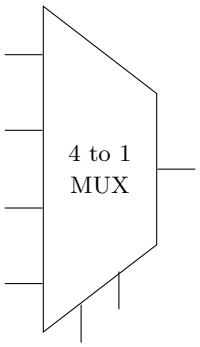




2. (15 points) Using only 2 to 1 multiplexers, draw a circuit diagram for a 5 to 1 MUX. Include a truth table.

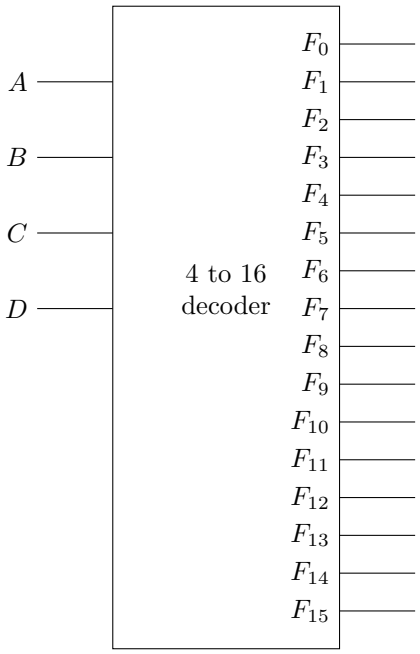
3. (20 points) Use a 4 to 1 MUX and a minimum number of external gates to realize the function $F(A, B, C, D) = \Sigma m(3, 5, 7, 12, 14) + \Sigma d(0, 1, 4, 6, 15)$. Draw a circuit diagram and write the corresponding MUX equation.

	AB			
CD	00	01	11	10
00				
01				
11				
10				

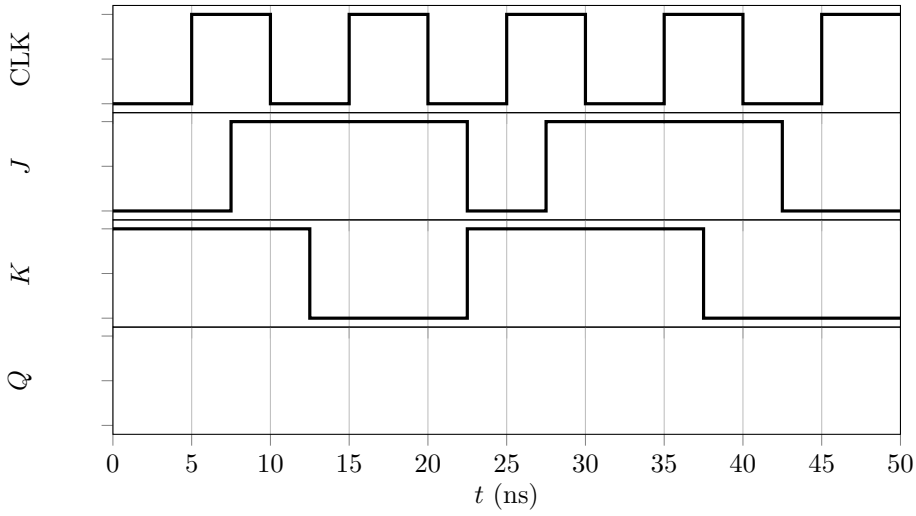


$F =$ _____

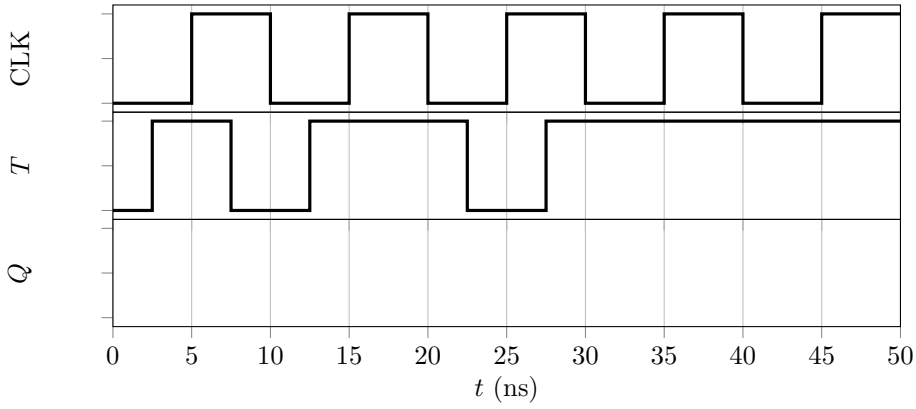
4. (15 points) Use the following 4 to 16 decoder and a minimum number of external gates to realize the function $F(A, B, C, D) = \Sigma m(1, 3, 5, 7, 12, 14) + \Sigma d(4, 8, 11, 13)$. (In other words, draw the circuit diagram below using the decoder inputs and/or outputs.) Assume that you have access to gates with only two inputs.



5. (15 points) Fill out the following timing diagram for a falling-edge triggered JK flip-flop. Ignore propagation delays. The value of Q is initially equal to 1.



6. (15 points) Fill out the following timing diagram for a rising-edge triggered T flip-flop. Ignore propagation delays. The value of Q is initially equal to 0.



7. (30 points) Design a 3-bit counter that counts in the sequence (001, 101, 010, 110, 000, 011...) using T flip-flops and a minimum number of external gates. Determine the logic required on the input of each flip-flop, then draw the circuit diagram.

A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						