

Name: SOLUTIONS

Read each question carefully before answering. Answer all parts. Show all work, calculations, and/or reasoning, otherwise no points will be awarded. Properly labeled loops **must be shown** on K-maps to receive credit. Assume that you have access to gates with as many inputs as you need. Point values are as indicated. Usage of XOR and XNOR gates is **not allowed** on this exam!

1. (10 points) Use a K-map to find the **minimum POS** implementation for the following expression. Label all loops or no credit will be awarded.

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 5, 6, 12, 14, 15)$$

	AB			
CD	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	1	0	1	0
10	0	1	1	0

Handwritten annotations on the K-map:

- Loop 1: $(B+D)$ (Covers cells (00,00), (01,00), (11,00), (10,00))
- Loop 2: $(A'+C+D')$ (Covers cells (01,01), (11,01), (01,11), (11,11))
- Loop 3: $(A'+B)$ (Covers cells (01,11), (11,11), (01,10), (11,10))
- Loop 4: $(A+B'+C'+D')$ (Covers cells (00,00), (01,00), (00,10), (01,10))

$$F_{\text{POS}} = (B+D)(A'+C+D')(A'+B)(A+B'+C'+D')$$

2. (10 points) Use a K-map to find the **minimum SOP** implementation for the following expression. Label all loops or no credit will be awarded.

$$F(A, B, C, D, E) = \Sigma m(1, 5, 8, 9, 13, 18, 19, 24, 25, 28, 29) + \Sigma d(2, 3, 14, 21, 22, 30)$$

DE	000	001	011	010	110	111	101	100
00	0	0	0	1	1	1	0	0
01	1	1	1	1	1	1	X	0
11	X	0	0	0	0	0	0	1
10	X	0	X	0	0	X	X	1

Handwritten annotations on the K-map:

- A circle around the 1s in the 00 row is labeled $BC'D'$.
- A circle around the 1s in the 01 row is labeled ABC .
- A circle around the 1s in the 100 column is labeled ABD' .
- A circle around the 1s in the 101 and 110 columns is labeled $B'C'D$.
- A circle around the 1s in the 100 and 101 columns is labeled $A'D'E$.

$$F_{SOP} = A'D'E + BC'D' + ABD' + B'C'D$$

3. (15 points) Use the Quine-McCluskey method to find a static-hazard free implementation of the following expression.

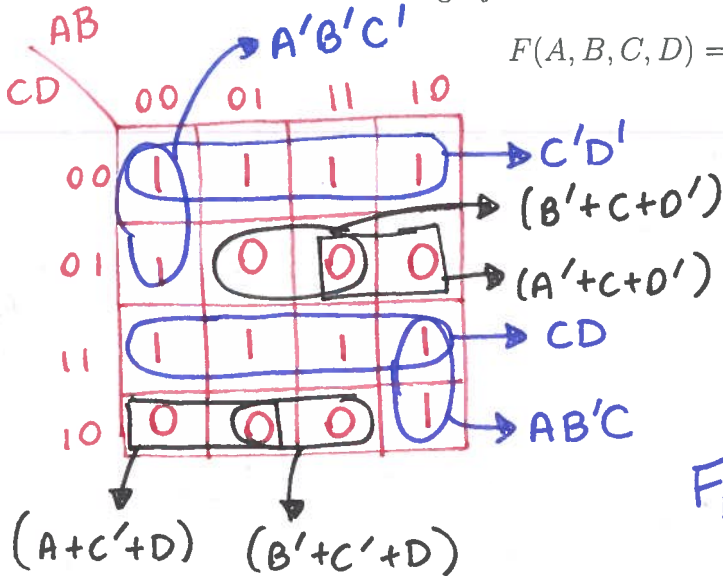
$$F(A, B, C, D, E) = \Sigma m(5, 12, 21, 23, 24, 28, 29, 31) + \Sigma d(6, 7, 14, 15)$$

	Column 1	Column 2	Column 3
TWO	✓ 5. 00101	✓ 5-7 001-1	5-7-21-23 -01-1
	✓ 6. 00110	✓ 5-21 -0101	5-21-15-23 repeat
	✓ 12. 01100	✓ 6-7 0011-	6-7-14-15 0-11- CARE
	✓ 24. 11000	✓ 6-14 0-110	6-14-7-15 repeat
		12-14 011-0	
THREE	✓ 7. 00111	12-28 -1100	7-15-23-31 --111
	✓ 14. 01110	24-28 11-00	7-23-15-31 repeat
	✓ 21. 10101	7-15 0-111	21-23-29-31 1-1-1
	✓ 28. 11100	7-23 -0111	21-29-23-31 repeat
		15-23 00000	
FOUR	✓ 15. 01111	✓ 4-15 0111-	
	✓ 23. 10111	✓ 21-23 101-1	
	✓ 29. 11101	✓ 21-29 1-101	
FIVE	^{PIs} ✓ 31. 11111	28-29 1110-	
		✓ 15-31 -1111	
		✓ 23-31 1-111	
		✓ 29-31 111-1	

$$F_{\text{HAZARD-FREE}} = A'BCE' + BCD'E' + ABD'E' + ABCD' + B'CE + CDE + ACE$$

4. (20 points) Find the lowest cost implementation of the following expression. Draw the circuit diagram of the minimum-cost circuit. Use any minimization method of your choice, showing all work and making a justification for the best implementation.

$$F(A, B, C, D) = \Pi M(2, 5, 6, 9, 13, 14)$$



$$F_{\text{SOP}} = C'D' + A'BC' + CD + AB'C$$

5 GATES
14 INPUTS

$$F_{\text{SOP}} = C'(D' + A'B') + C(D + AB')$$

7 GATES
14 INPUTS

OR

$$C'D' + CD + B'(A'C' + AC)$$

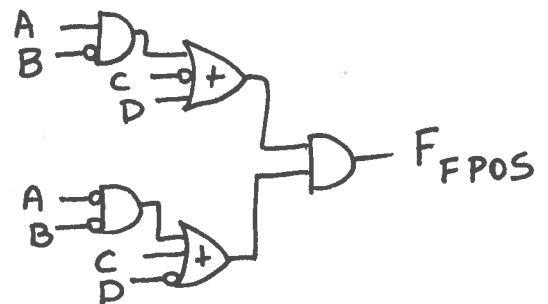
6 GATES
14 INPUTS

$$F_{\text{POS}} = (A + C' + D)(B' + C' + D)(A' + C + D')(B' + C + D')$$

5 GATES
16 INPUTS

$$F_{\text{POS}} = (D + C' + AB')(C + D' + A'B')$$

5 GATES
12 INPUTS
LOWEST COST CIRCUIT



5. Find the optimized implementation of the following two circuits. Show all work. How many gates and/or inputs do you save by implementing circuits together rather than individually?

$$X(A, B, C, D) = \Sigma m(2, 3, 4, 6, 7, 10, 12)$$

$$Y(A, B, C, D) = \Sigma m(4, 6, 7, 10, 12, 14, 15)$$

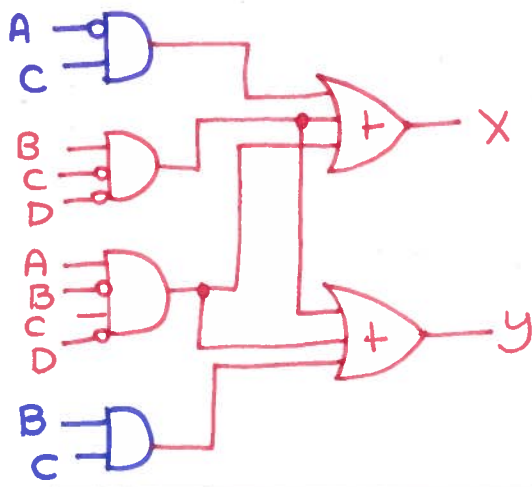
X		AB				Y		AB			
CD		00	01	11	10	CD		00	01	11	10
00	0	0	1	1	0	00	0	0	1	1	0
01	0	0	0	0	0	01	0	0	0	0	0
11	1	1	0	0	0	11	0	1	1	0	0
10	1	1	0	1	1	10	0	1	1	1	1

A'C

BC'D'

AB'CD'

BC



6 GATES
17 INPUTS

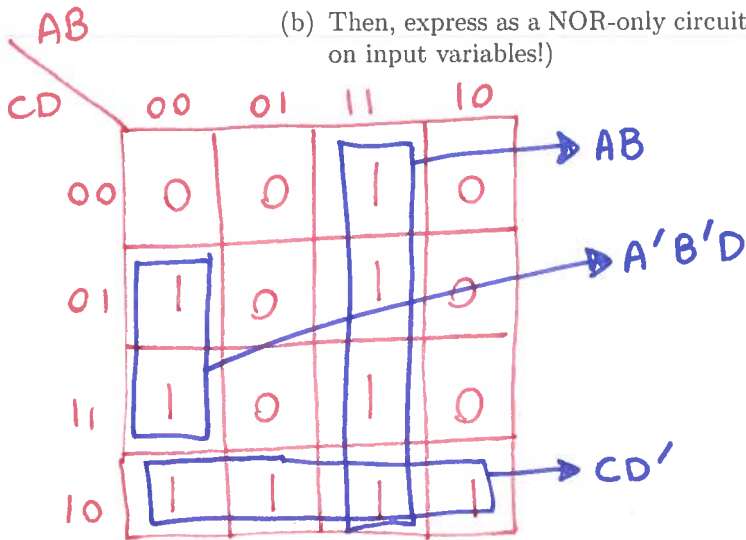
THIS SAVES
2 GATES &
4 INPUTS!

INDIVIDUALLY
 $X = A'C + BC'D' + B'CD'$
 $Y = BC + BD' + ACD'$
 NO SHARED GATES

6. (15 points) Find the **minimum SOP** implementation of the following expression.

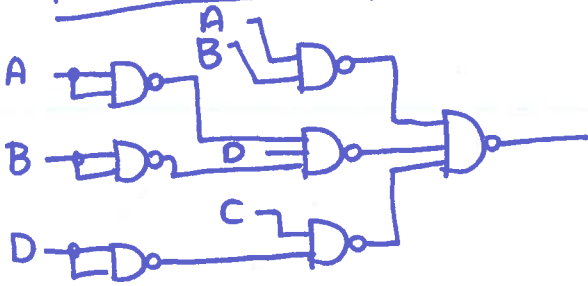
$$F(A, B, C, D) = \Sigma m(1, 2, 3, 6, 10, 12, 13, 14, 15)$$

- (a) Then, express as a NAND-only circuit (no inverters are allowed, not even bubbles or primes on input variables!)
- (b) Then, express as a NOR-only circuit (no inverters are allowed, not even bubbles or primes on input variables!)

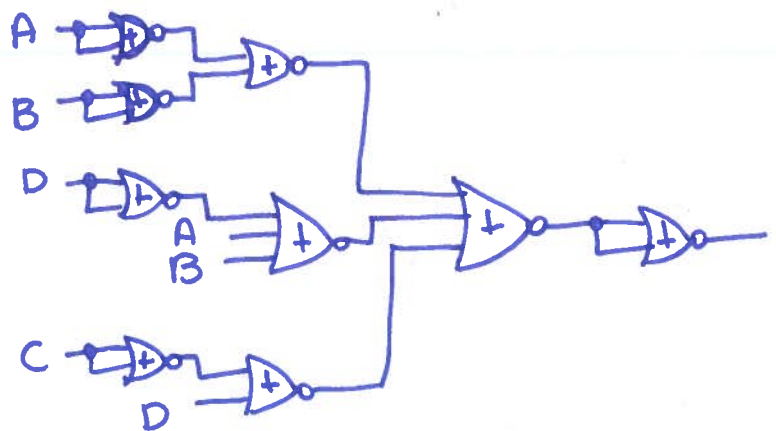


$$F_{SOP} = AB + A'B'D + CD'$$

NAND-ONLY



NOR-ONLY



7. (10 points) Draw a timing diagram for the following circuit, given gate delays of 2 ns for NOT gates, and 5 ns for AND and OR gates. Indicate any static hazards in the output signal

