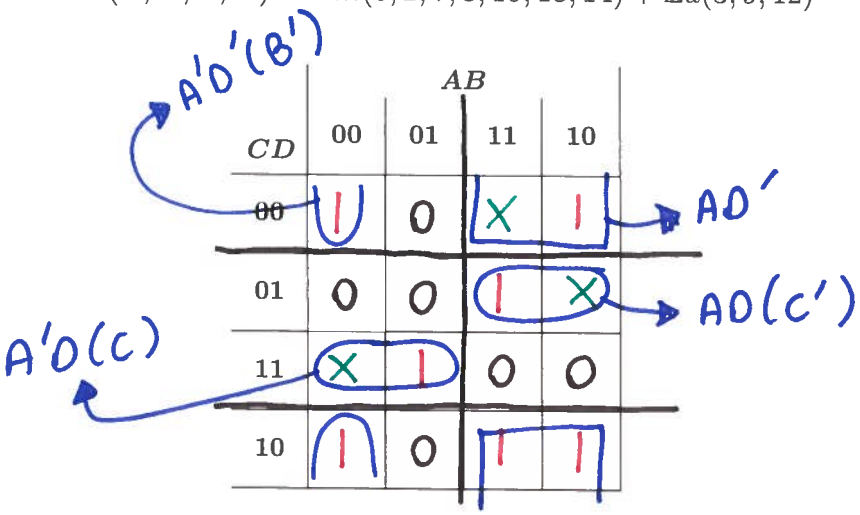
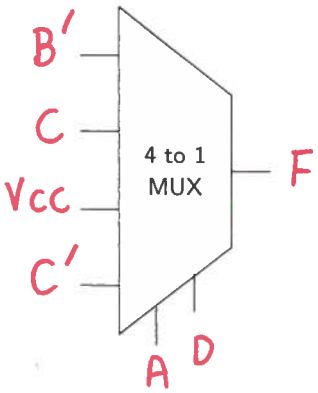
Name: FALL 2017 SOLUTIONS

Read each question carefully before answering. Answer all parts. Show all work, calculations, and/or reasoning, otherwise no points will be awarded. Properly labeled loops must be shown on K-maps. Point values are as indicated.

1. (10 points) Implement the following minterm expression with a 4 to 1 MUX and a minimum number of external gates. Include the MUX equation and properly label the circuit diagram.

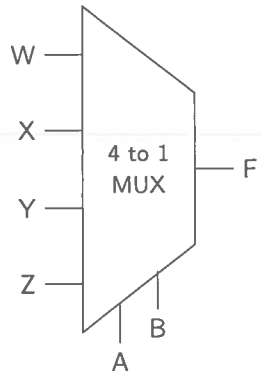
$$F(A,B,C,D) = \Sigma m(0,2,7,8,10,13,14) + \Sigma d(3,9,12)$$

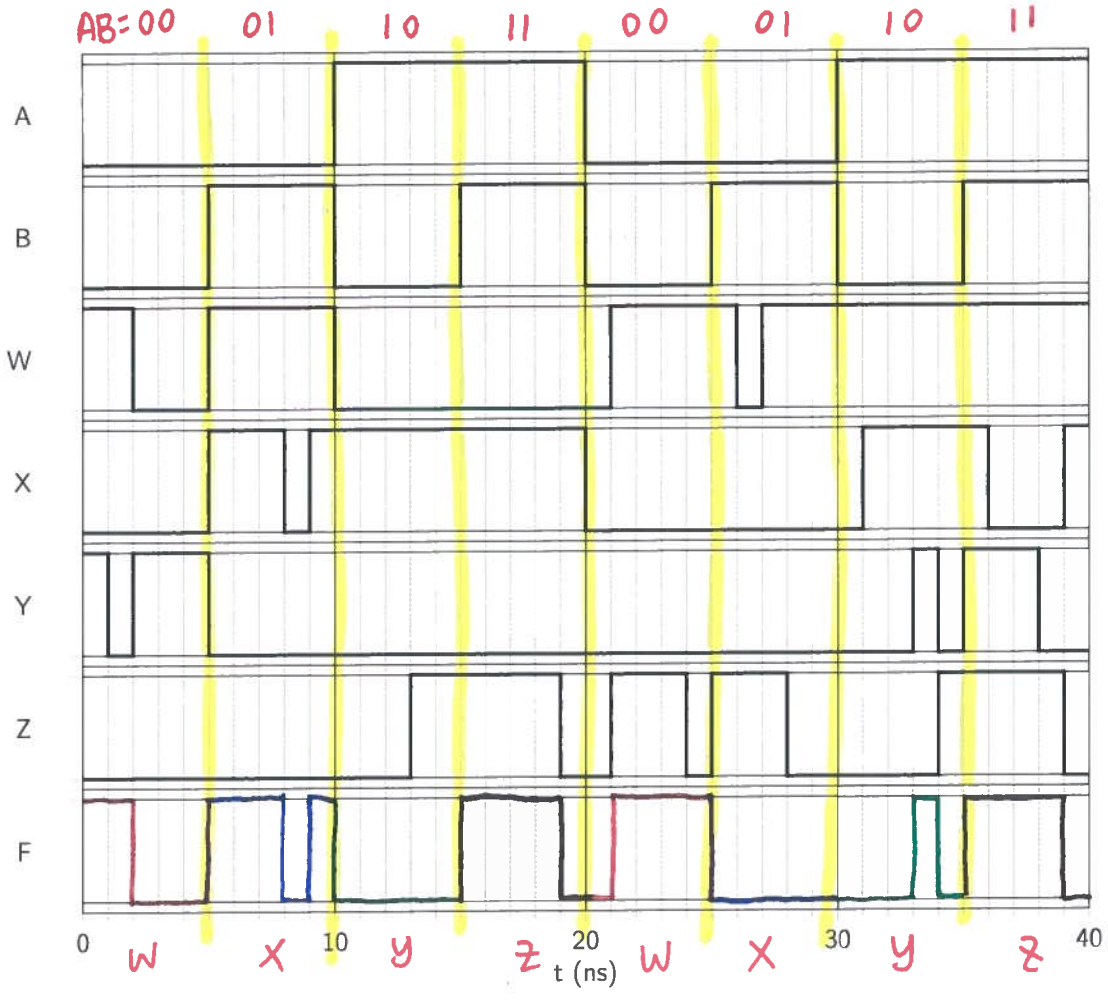




$F =$ A'D'(B') + A'D(C) + AD'(1) + AD(C')

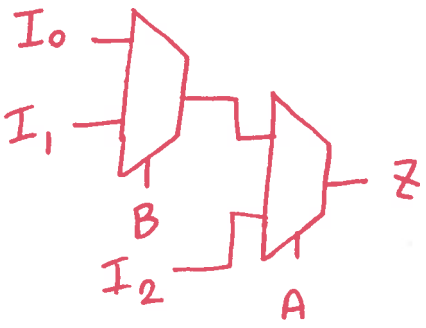
2. (10 points) Fill out the following timing diagram for the output F of the given 4 to 1 MUX. Ignore all gate delays.



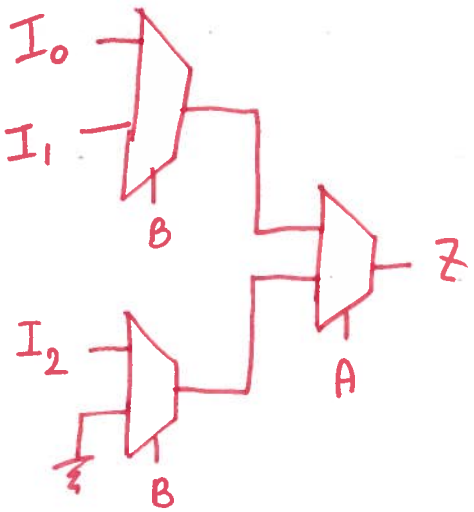


3. (10 points) Design a 3 to 1 MUX using only 2 to 1 multiplexers. Include a truth table and a circuit diagram of your multiplexer design.

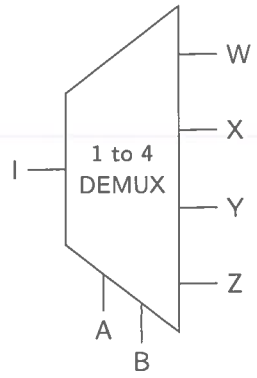
A	B	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	X

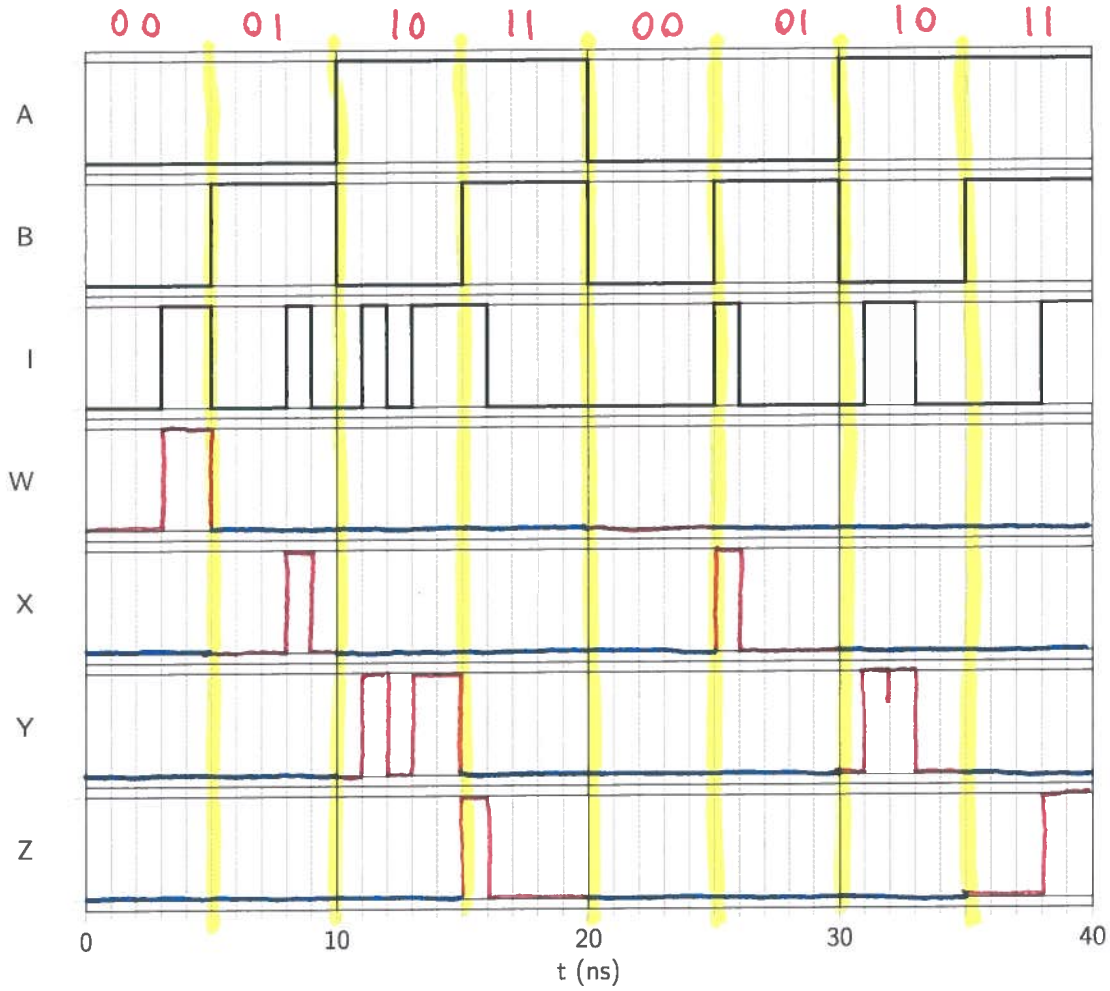


-OR-



4. (10 points) Fill out the following timing diagram for the outputs W, X, Y, and Z of the given 1 to 4 DEMUX. Ignore all gate delays.



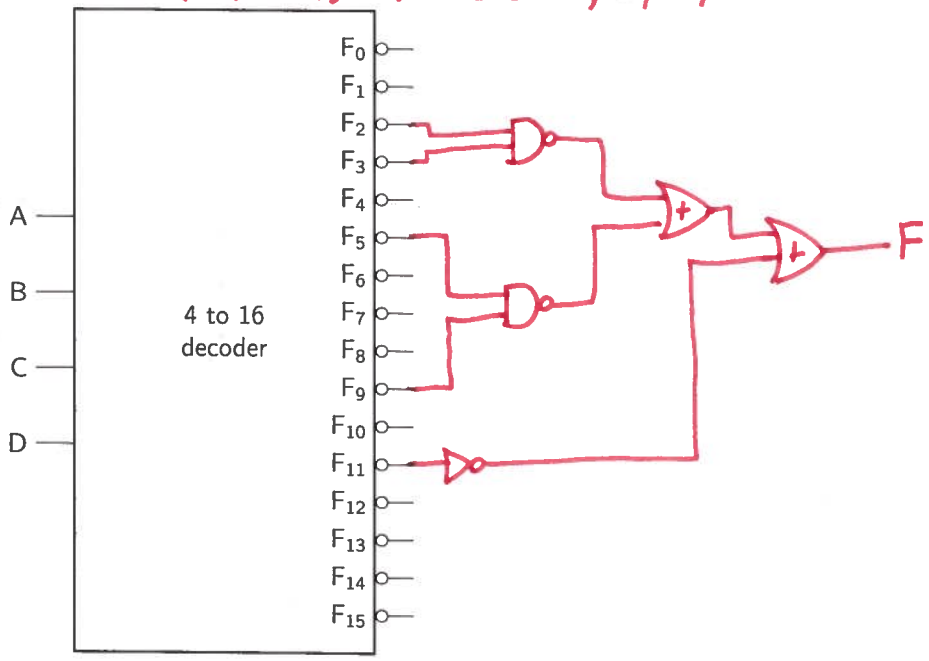


5. (10 points) Use the outputs from the following 4 to 16 decoder and a minimum number of **2-input** external gates to realize the following Maxterm expression. Properly label the circuit diagram.

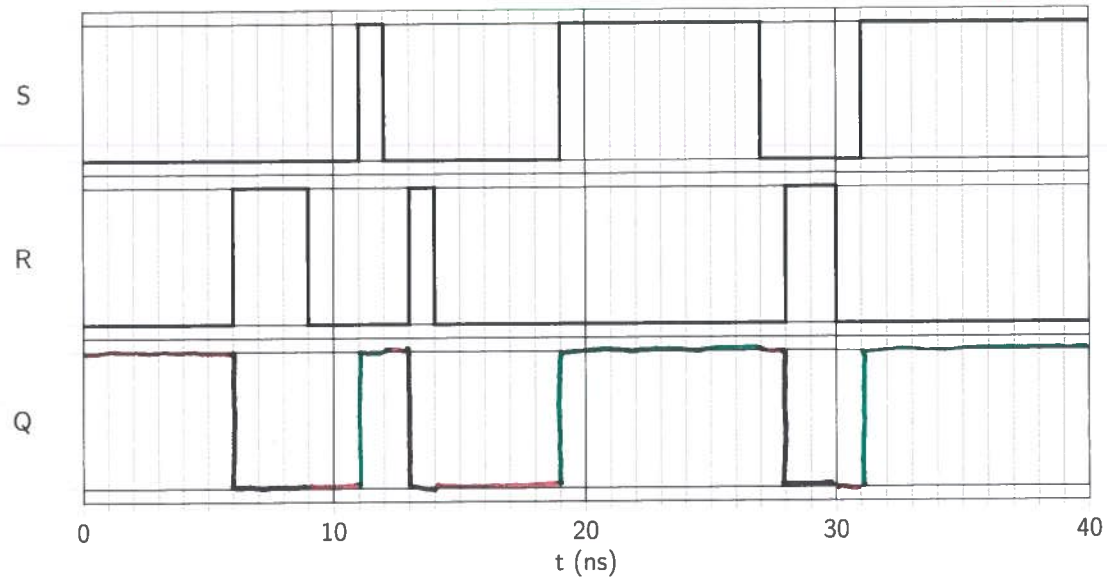
oops!

$$F(A,B,C,D) = \Pi M(0,4,6,10,13,14,15) + \Pi D(1,7,8,12)$$

$$= \Sigma m(2,3,5,9,11) + \Sigma d(1,7,8,12)$$

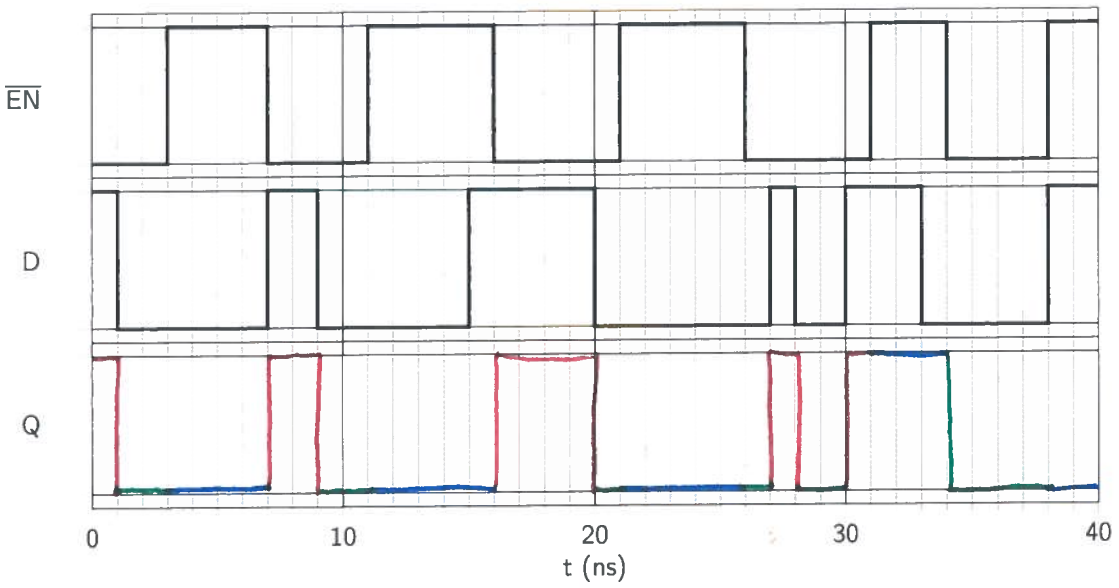


6. (10 points) Fill out the following timing diagram for an SR latch. Ignore all gate delays. Q(0) = 1.



0-6 ns HOLD
6-9 ns RESET
9-11 ns HOLD
11-12 ns SET
12-13 ns HOLD
13-14 ns RESET
14-19 ns HOLD
19-27 ns SET
27-28 ns HOLD
28-30 ns RESET
30-31 ns HOLD
31-40 ns SET

7. (10 points) Fill out the following timing diagram for an active-low gated D latch. Ignore all gate delays. Q(0) = 0.

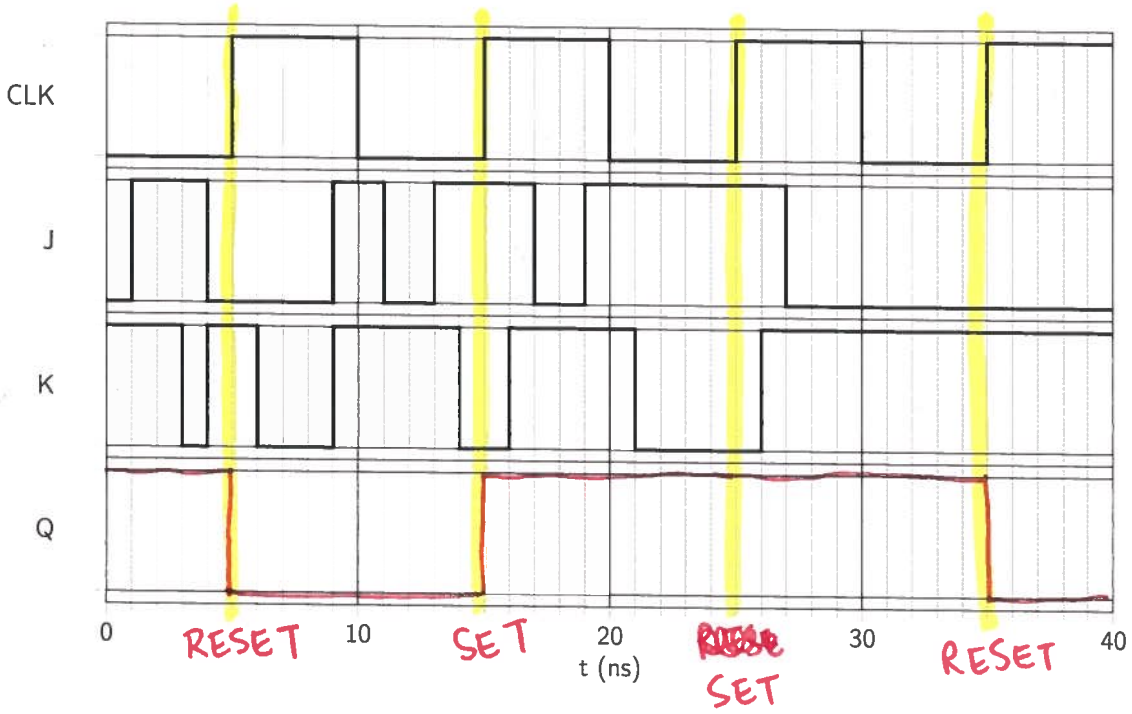


NOT ENABLED: 3-7 ns, 11-16 ns, 21-26 ns, 31-34 ns, 38-40 ns

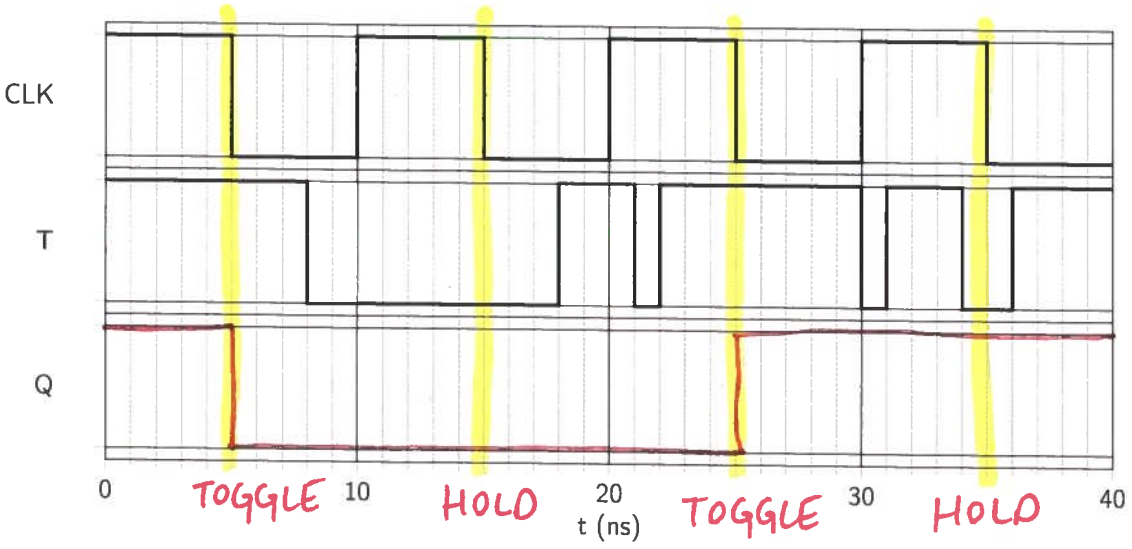
SET: WHEN $\overline{EN}=0$ AND D=1

RESET: WHEN $\overline{EN}=0$ AND D=0

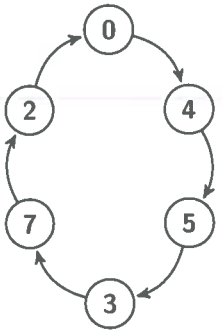
8. (10 points) Fill out the following timing diagram for a rising-edge triggered JK flip-flop. Ignore all gate delays. $Q(0) = 1$.



9. (10 points) Fill out the following timing diagram for a falling-edge triggered T flip-flop. Ignore all gate delays. $Q(0) = 1$.



10. (10 points) Design a 3-bit counter that counts in the sequence given in the state diagram below. Use T flip-flops and a minimum number of external gates. Write each flip-flop equation, then draw the circuit diagram using the template below.

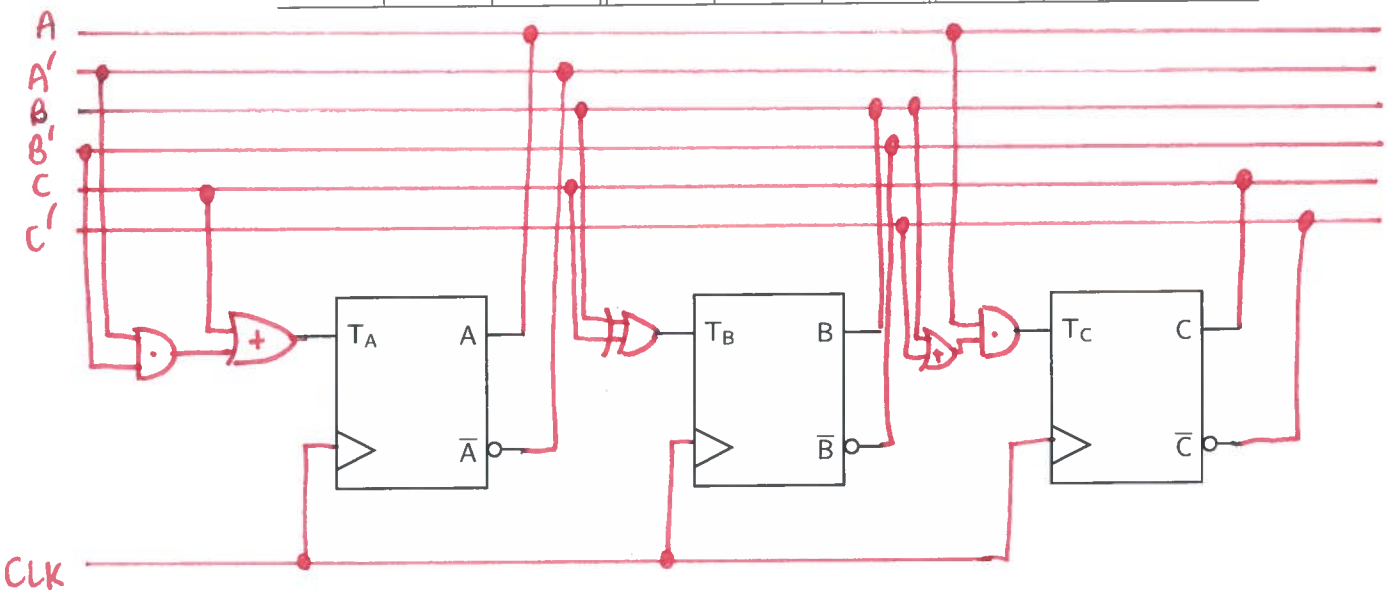


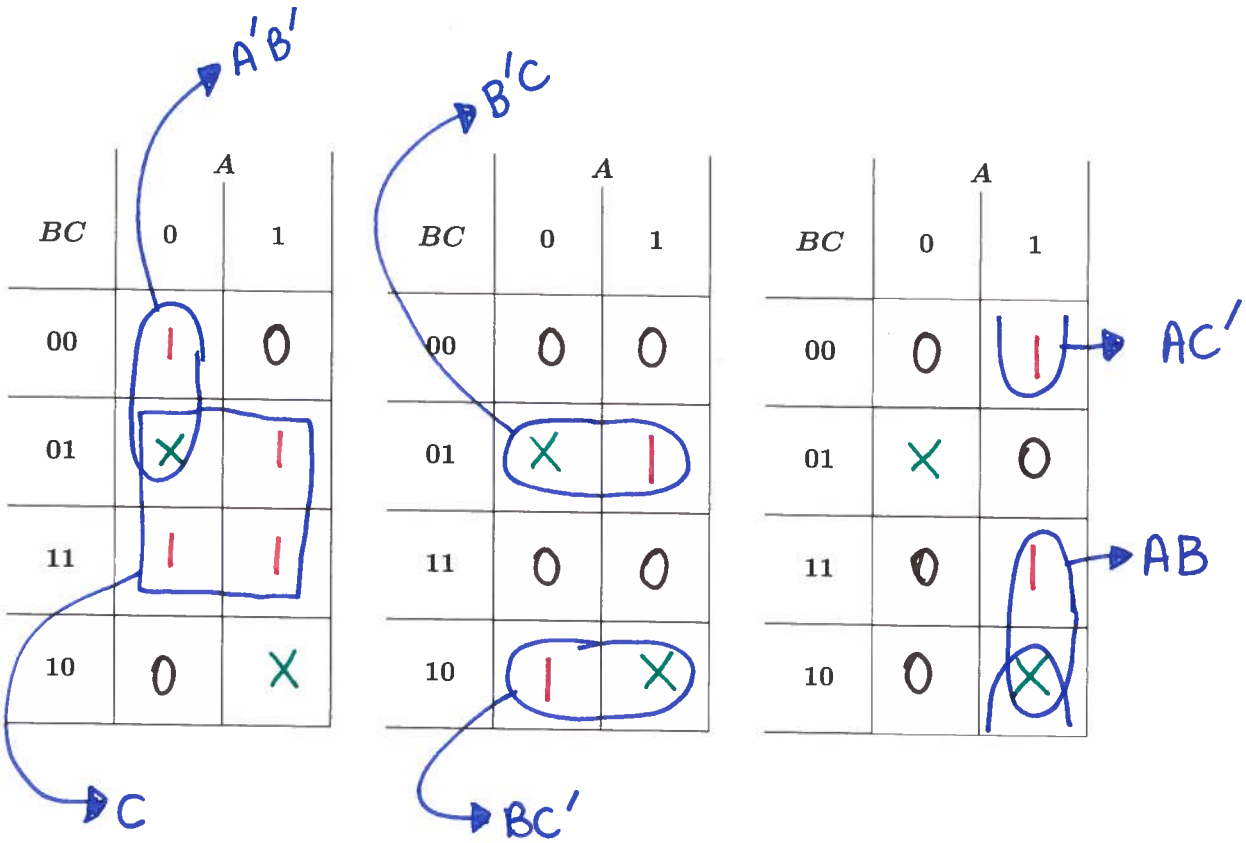
$T_A = A'B' + C$

$T_B = B \oplus C$

$T_C = A(B + C')$

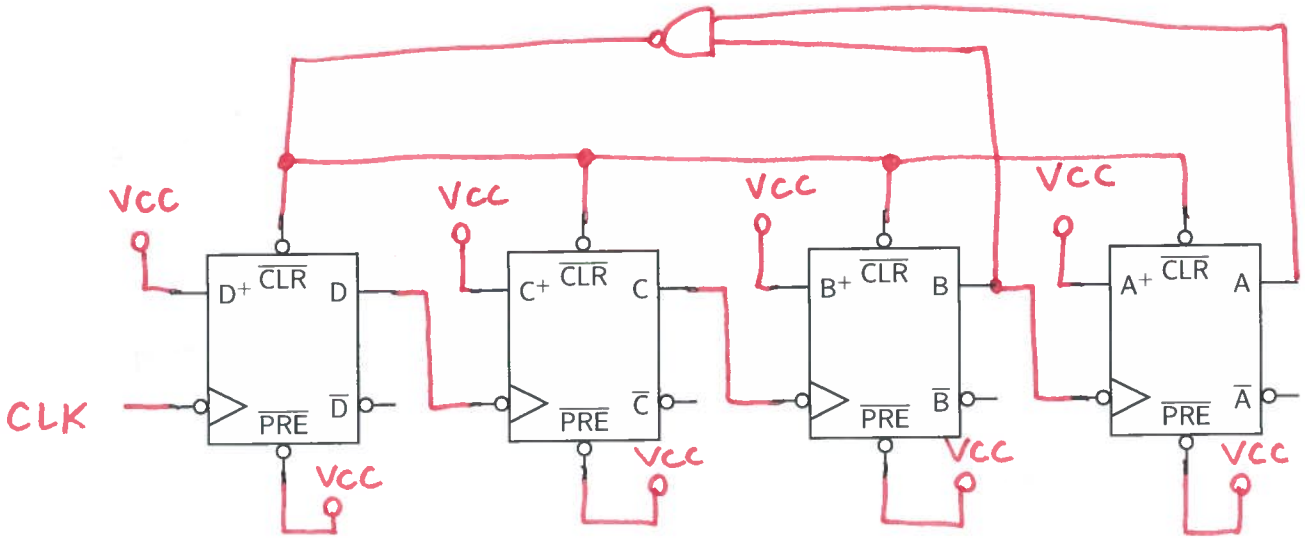
A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	1	0	0	1	0	0
0	0	1	X	X	X	X	X	X
0	1	1	1	1	1	1	0	0
0	1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0	1
1	0	1	0	1	1	1	1	0
1	1	1	0	1	0	1	0	1
1	1	0	X	X	X	X	X	X




A'B'
C
B'C
BC'
AC'
AB
A
BC
0
1
00
01
11
10

11. (10 points) Design a 4-bit ripple counter that counts from 0–11. Use either D or T flip-flops (indicate which you choose) and a minimum number of external gates. Draw the circuit diagram using the template below. The flip-flop labeled A corresponds to the MSB of the counter, and the flip-flop labeled D corresponds to the LSB of the counter.

Flip-Flop Type: T

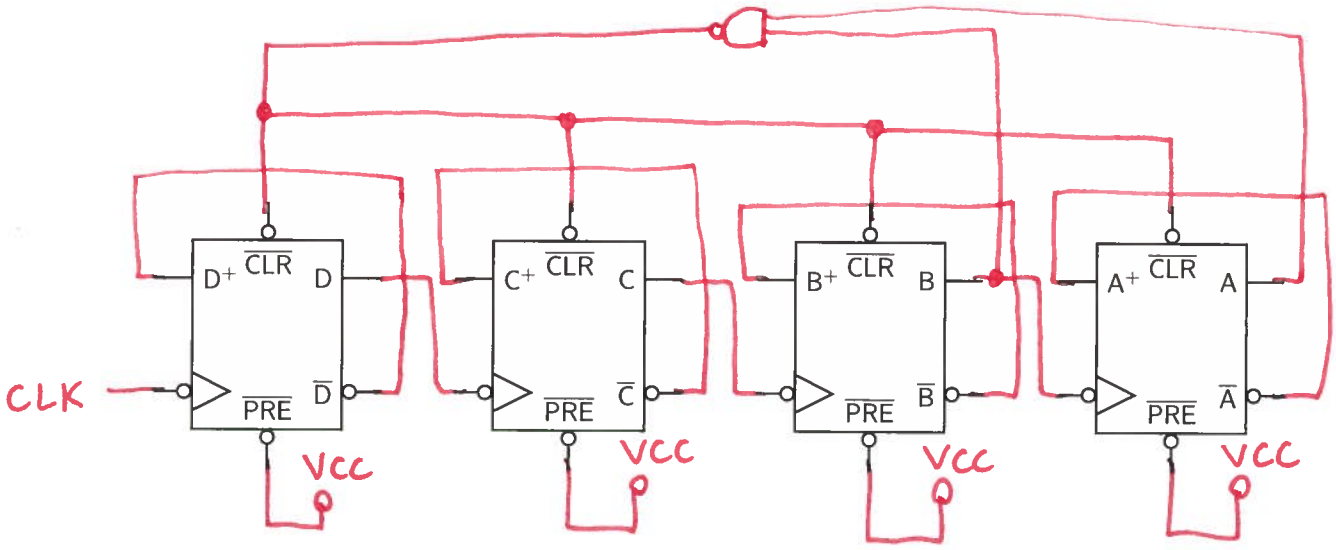


$\overline{CLR}$ must go to zero when A & B are both 1. therefore

$$\overline{CLR} = \overline{AB}$$

11. (10 points) Design a 4-bit ripple counter that counts from 0–11. Use either D or T flip-flops (indicate which you choose) and a minimum number of external gates. Draw the circuit diagram using the template below. The flip-flop labeled A corresponds to the MSB of the counter, and the flip-flop labeled D corresponds to the LSB of the counter.

Flip-Flop Type: D



$\overline{CLR}$ must go to zero when A & B are both 1. Therefore

$$\overline{CLR} = \overline{AB}$$