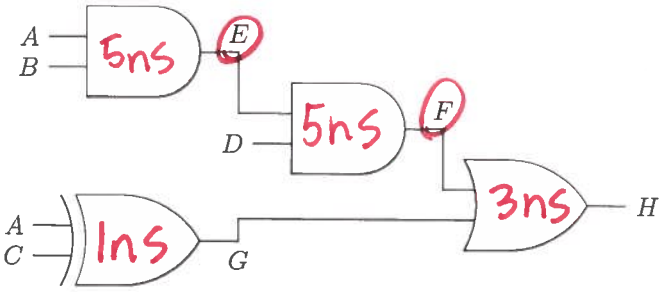
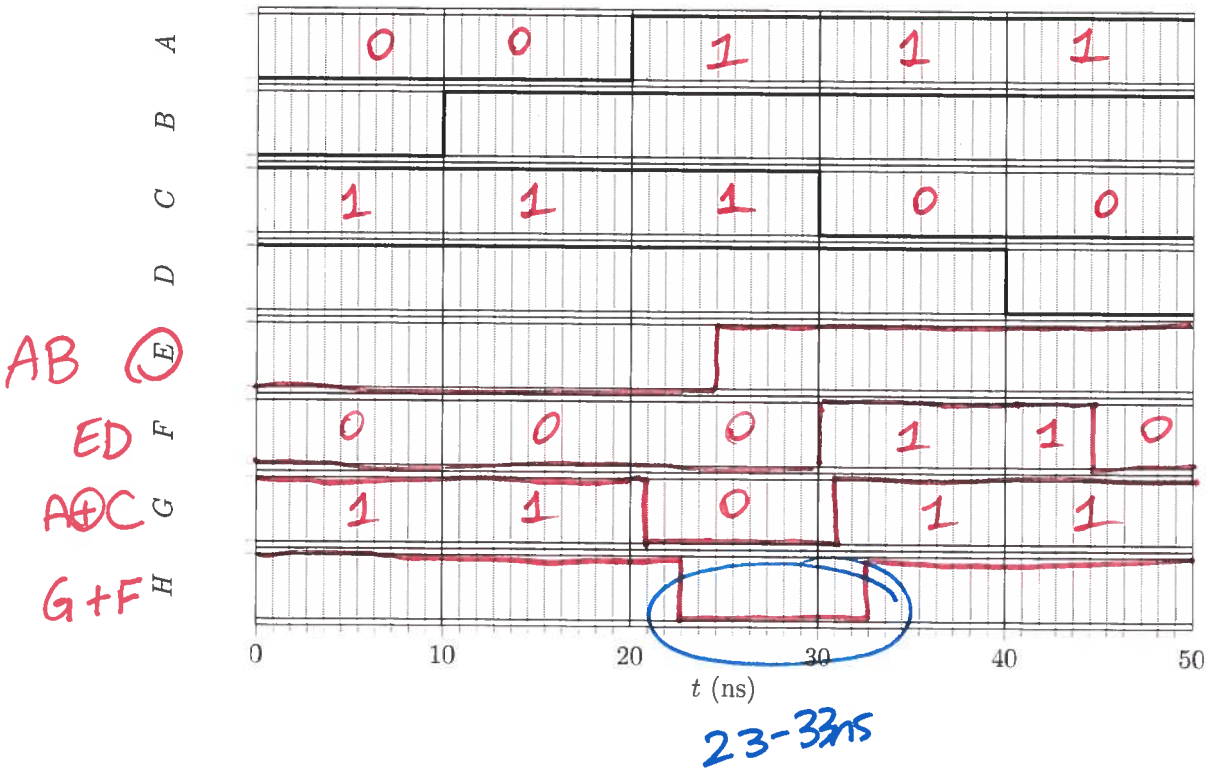
Name: SOLUTIONS

Read each question carefully before answering. Answer all parts. Show all work, calculations, and/or reasoning, otherwise no points will be awarded. Properly labeled loops must be shown on K-maps. Point values are as indicated.

1. (25 points) Given the following circuit diagram, fill out the timing diagram for E, F, G and H given the values of inputs A, B, C, and D. Indicate any hazards, given that H *should* be logic HIGH the entire duration of this timing diagram. Each XOR gate has a delay of 1 ns, each AND gate has a delay of 5 ns, and each OR gate has a delay of 3 ns.





AB (E)

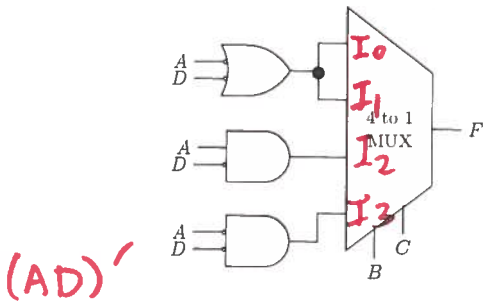
ED

A⊕C

G+F

23-33ns

2. Your buddy (who may or may not be any good at digital systems), shows you the following diagram of a circuit they wired up.



(AD)′ (A+D)′

(a) (5 points) What is the MUX equation corresponding to the above circuit?

$F =$ B'C'(A'+D') + B'C(A+D') + BC'(AD') + BC(A'D')

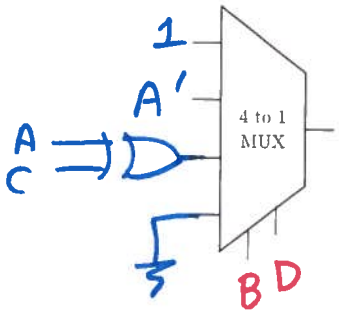
(b) (5 points) Fill out the following K-map based on the above equation.

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	0	0	0
11	1	0	0	0
10	1	1	0	1

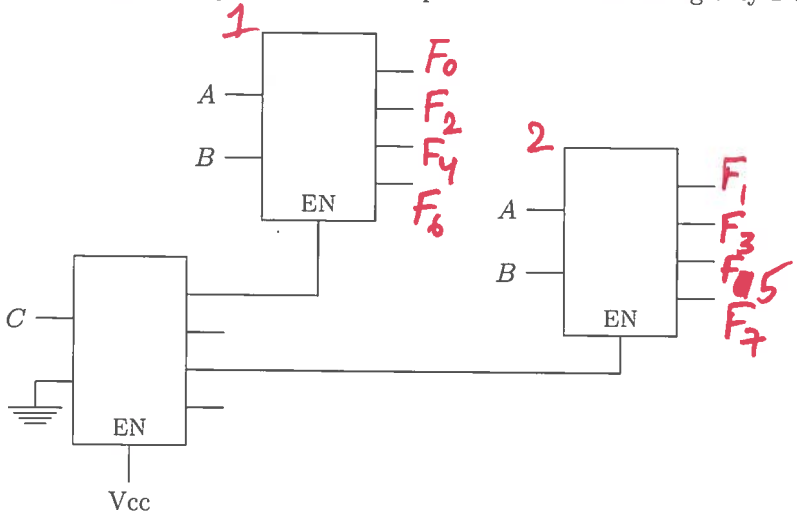
B'D'(1) + B'D(A') + BD'(A⊕C) + BD(0)

(c) (10 points) Find a MUX implementation of this circuit that requires a minimum number of gates. Write the MUX equation and fill out the corresponding circuit diagram.

$F =$ _____



3. Your buddy from question 2 wired up a 3 to 8 decoder using only 2 to 4 decoders as follows.

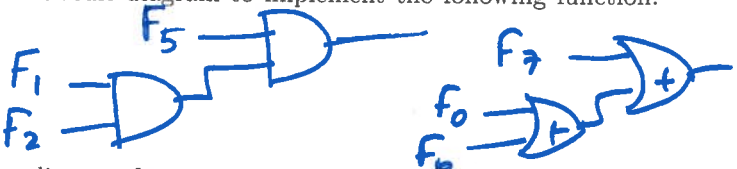


A B C
F_0 0 0 0
F_1 0 0 1
F_2 0 1 0

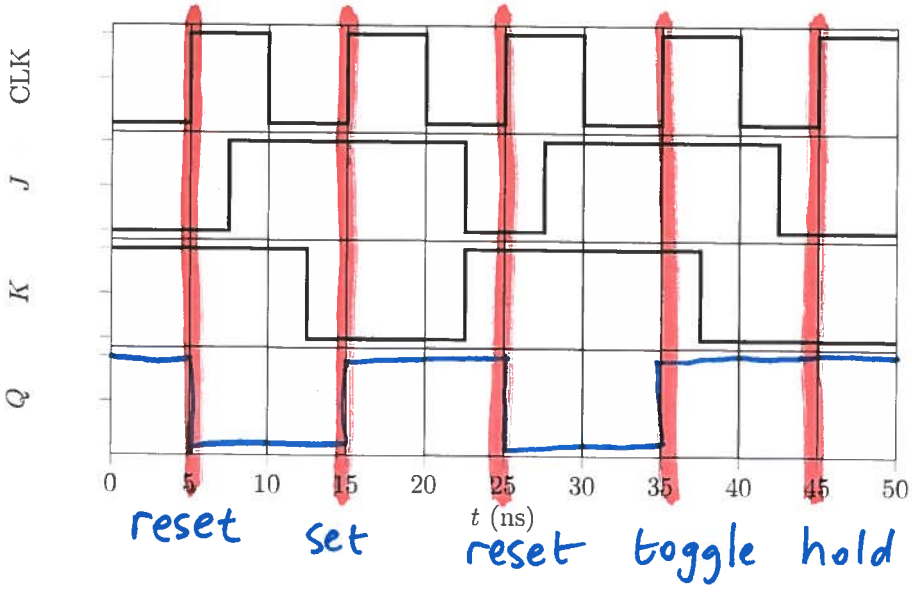
(a) (7 points) Label the above circuit diagram with outputs from F_0 – F_7.

(b) (3 points) Using only the decoder outputs, and a minimum number of **2-input gates**, use the above schematic to draw a circuit diagram to implement the following function: $\Pi M(1,2,5) + \Pi D(3,4)$.

$\Sigma m(0,6,7)$



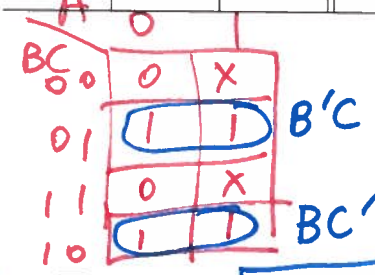
4. (10 points) Fill out the following timing diagram for a rising-edge triggered JK flip-flop. Ignore propagation delays. The value of Q is initially equal to 1.

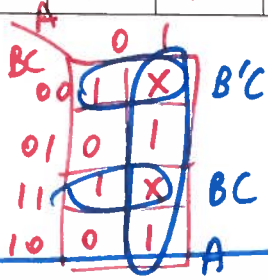


1 5 2 6 0 3

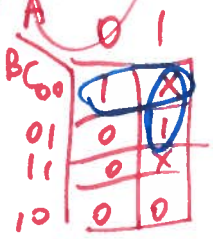
5. (30 points) Design a 3-bit counter that counts in the sequence (001, 101, 010, 110, 000, 011...) using T flip-flops and a minimum number of external gates. Determine the logic required on the input of each flip-flop, then draw the circuit diagram using the template below.

A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	0	1	1	0	1	1
0	0	1	1	0	1	1	0	0
0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	0	1	0
1	0	0	X	X	X	X	X	X
1	0	1	0	1	0	1	1	1
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X





A+B'⊕C



B'C'+
B'A
B'(A+C')